ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor integrated circuit which assures sufficiently lower power consumption of a translation look-aside buffer without deterioration of operation rate performance thereof.

In the translation look-aside buffer to convert logical address into physical address, a clock enable generating circuit is provided to stop the operation clock to be supplied to the tag memory and entry memory of the translation look-aside buffer while the virtual memory valid bit Vs of the status register indicating access to the virtual memory is "0", or while the cache-stall signal is outputted because of miss-hit in the cache, or when the access is issued with the same logical page address to the area other than the boundary area of the address range.